CLAIMS:

1. A method for iterative decoding comprising:

generating an output based on a received coded signal using a first soft-input soft-output device having a first trellis structure; and

processing the output in an iterative loop using a second soft-input soft-output device having a second trellis structure.

2. The method of claim 1 further comprising:

receiving a coded signal from a communication channel prior to generating an output.

3. The method of claim 2, wherein the communication channel is a channel on a hard disc of a computer.

4. The method of claim 1, wherein the second trellis structure represents fewer states than the first trellis structure

5. The method of claim 1, wherein before processing the output, the method further comprising:

improving the output with a third SISO device having a third trellis structure that represents fewer states than the first trellis structure.

6. The method of claim 1, wherein the first trellis structure and the second trellis structure represent factors of a mathematical model representative of at least a communication channel and a precoder.

7. A method of operating a turbo decoding circuit for decoding a received signal from a channel which can be represented by a mathematical model that is a convolution of two or more equations, one of the two or more equations being a complicated equation, the method comprising:

processing the received signal with a first SISO device having a trellis structure corresponding to state-outputs of the complicated equation; and

processing an output of the first SISO device with one or more secondary SISO devices corresponding to state-

outputs of each remaining equation of the two or more equations; and

iteratively decoding an output of the one or more secondary SISO devices corresponding to state-outputs of each remaining equation.

8. The method of claim 7, wherein the step of processing the received signal comprises:

inputting the received signal into the first SISO device; and

generating from the first SISO device a soft-output corresponding to the received signal.

9. The method of claim 7, wherein the step of processing an output of the first SISO device comprises:

inputting the output of the first SISO device into one or more secondary SISO devices; and

generating a soft-output based on the output of the first SISO device.

10. The method of claim 7, wherein iteratively decoding comprises:

inputting a soft-output output of the one or more secondary devices into a de-interleaver; and

passing the de-interleaved soft-outputs to a decoder.

11. The method of claim 10, wherein iteratively decoding further comprises:

subtracting a de-interleaved soft-output from the one or more secondary SISO devices from an output of the decoder to form a difference value;

interleaving the difference value; and

inputting the interleaved difference value into the one or more secondary SISO devices as a secondary input; and

subtracting the interleaved value from the soft-output of the one or more secondary SISO devices.

12. The method of claim 7, wherein iteratively decoding comprises:

rendering soft-ouputs in one of four states based the output received from the first SISO device.

13. An apparatus for turbo decoding coded information received from a channel, the apparatus comprising:

a first SISO device having a first trellis structure, the first SISO device for receiving the coded information; and

a decoder loop having a second SISO device with a second trellis structure, the decoder loop for receiving a soft-output from the first SISO device and for iteratively generating an output value representative of the received coded information.

14. The apparatus of claim 13 wherein the decoder loop further comprises:

a decoder device;

a de-interleaver in communication with the decoder and second SISO device; and

an interleaver in communication with the decoder and the second SISO device.

15. The apparatus of claim 13 wherein the channel is a track on a hard disc drive.

16. The apparatus of claim 13 wherein the first SISO device has a state trellis structure corresponding to the complex factor of the mathematical model.

17. The apparatus of claim 13 wherein the first SISO device has more possible states than the second SISO device.

18. The apparatus of claim 13 wherein the second SISO device has a state trellis structure corresponding to the simple factor.

19. The apparatus of claim 18 wherein the second SISO device is capable of generating a soft output according to the received coded information.

20. The apparatus of claim 13 wherein the decoder loop is implemented in a parallel architecture in a circuit.

21. The apparatus of claim 13 wherein the first trellis structure of the first SISO device is more complex than the second trellis structure of the second SISO device, and further comprising:

a third SISO device for receiving the soft-output directly from the first SISO device and for improving the soft output, wherein the second SISO device receives the soft-output from the first SISO device indirectly.

22. An apparatus for turbo decoding information comprising:

a first SISO device having a n-state trellis structure for receiving a coded signal and for generating an output bit and a reliability bit corresponding to the coded signal; and

a Turbo decoder loop having a second SISO device with a m-state trellis structure for receiving the output bit and the reliability bit and for iteratively generating a decoded output corresponding to the coded signal.

23. The apparatus of claim 22 wherein the Turbo decoder further comprises:

a decoder device;

an interleaver in communication with the decoder device and the second SISO device; and

a de-interleaver in communication with the decoder device and the second SISO device.

24. The apparatus of claim 22 wherein the information is received from a magnetic recording medium.

25. The apparatus of claim 22 wherein the first SISO device state trellis structure according to a chosen alphabet and a channel memory length.

26. The apparatus of claim 22 wherein wherein n is greater than m.

27. The apparatus of claim 22 wherein the decoder loop is implemented in a parallel architecture in a circuit.

28. The apparatus of claim 22 wherein the n-state trellis structure and the m-state trellis structure are representative of individual factors of a mathematical function representative of the channel.